

**REMARKS/ARGUMENTS**

Claims 43, 80, 82, 84-86, and 93-95 are amended. Claims 43, 48, 49, 51-57, 59-65, and 74-101 remain pending in the application. (Claims 44-47, 50, 58, and 66-73 were previously canceled.) Applicants respectfully request reexamination and reconsideration of the application in light of the following remarks.

Applicants wish to thank the Examiner for the courtesy extended to Applicants' representatives during an interview last November.

Claims 43, 48, 49, 51-57, 59-65, and 74-101 were rejected under 35 USC § 102(b) as anticipated by US Patent No. 5,012,187 to Littlebury ("Littlebury"). Applicants respectfully traverse this rejection.

Initially, Applicants clarify their statements in the Amendment mailed on November 8, 2004 (hereinafter the "November Amendment"). The pending claims are in product-by-process format. That is, the claims are directed to a product—a "tested semiconductor device"—claimed in terms of a process of producing the product. In traversing the rejection of the claims under 35 USC § 112, second paragraph made in the Office Action dated June 7, 2004, Applicants were merely pointing out that the pending claims do not impermissibly combine two claim formats (e.g., an apparatus and a process of using the apparatus), which is forbidden by *Ex parte Lyell*, 17 USPQ2d 1548 (Bd. Pat. App. & Inter. 1990). Rather, the pending claims are drafted in product-by-process format, which is a long recognized and permitted claim format and is not objectionable under 35 USC § 112, second paragraph.

As set forth in the MPEP, "[E]ven though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. . . . If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." (MPEP § 2113 (quoting *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985).) "Once the examiner provides a rationale tending to show that the claimed product appears to be the same or similar to that of the prior art, although produced by a different process, the burden shifts to applicant to come forward with evidence establishing an unobvious difference between the claimed product and the prior art." (MPEP § 2113.) Of course, if applicant does so, the claims are patentable over the prior art.

Here, the Examiner did his initial duty: the Examiner provided a rationale that allegedly shows that the claimed semiconductor die is the same as the semiconductor die disclosed in Littlebury. In response, as discussed in detail below, Applicants now come forward with argument and evidence that the process recited in the claims of this application gives rise to structural differences in the resulting tested semiconductor device as compared to prior art semiconductor dies like Littlebury.

Exhibit 1 attached hereto illustrates a depiction of exemplary probe elements attached to an exemplary probe substrate. In Figure A, the probe elements and the terminals of a semiconductor device are apart. In Figure B, the probe elements and/or the terminals are moved and brought into contact with each other. As shown in Figure C, the probe elements and/or the terminals can be moved past first contact so that the probe elements compress and exert forces against the terminals. Such a force can aide in creating electrical connections between the probe elements and the terminals. Typically, the probe elements create marks, which are often called scrub marks, on the terminals, and the size of each scrub mark is typically proportional to the force exerted by a probe element against the terminal.

Because of the "adjusting a planar orientation of probe elements of a probe card assembly to correspond to a planar orientation of said electrical contact terminals" recited in claim 43, the probe elements of claim 43 can be adjusted to be generally co-planar with respect to the terminals of the semiconductor device prior to effecting contact between the probe elements and the terminals. For this reason, the forces exerted by the probe elements against the terminals will be generally similar from probe to probe. Consequently, the scrub marks made by the probe elements will be generally uniform from terminal to terminal as depicted in Figure D. (Figure D shows a top view of the semiconductor device, which is shown in side view in Figures A-C.)

In contrast, a semiconductor device tested using a process that does not include "adjusting a planar orientation of probe elements of a probe card assembly to correspond to a planar orientation of said electrical contact terminals" will have irregular scrub marks from terminal to terminal. Figures E-G in Exhibit 2 (which is attached hereto) show probe elements that are out of planarity with terminals of a semiconductor device. As a result, the probe element on the left hand side in Figures E-G is the first probe element to contact a terminal, and the probe element on the right hand side is the last probe element to contact a terminal, as shown in Figure F. As shown in Figure G, as all of the probe elements are brought into contact with the

terminals, the probe elements on the left hand side are compressed to a greater degree than the probe elements on the right hand side, which means each probe element exerts a different level of force against a terminal. As shown in Figure H (which shows a top view of the semiconductor device), the resulting pattern of scrub marks left on the terminals is not uniform. Rather, the probes that exerted larger forces leave larger scrub marks. The resulting pattern can be a pattern of increasingly larger scrub marks from the right-most terminal moving toward the left-most terminal.

Littlebury discloses no mechanism for adjusting an orientation of probes 17 to correspond to an orientation of the terminals 13 of chips 12A, 12B. Rather, Littlebury relies solely on the flexibility of membrane 16 to compensate for misorientation of probes 17 and terminals 13 as the probes 17 are brought into contact with the terminals 13. Thus, in Littlebury, ones of probes 17 will contact ones of terminals 13 at different times with effects similar to what is shown in attached Exhibit 2. Littlebury's dies will thus have less uniform, less regular scrub marks.

Thus, the tested semiconductor device of claim 43 is structurally different than a semiconductor device tested using a prior art process—e.g., the dies disclosed in Littlebury—that lacks the "adjusting a planar orientation of probe elements of a probe card assembly to correspond to a planar orientation of said electrical contact terminals" recited in claim 43. That is, the tested semiconductor device of claim 43 has a more uniform, regular pattern of scrub marks on its terminals; in contrast, a prior art semiconductor device—like the dies in Littlebury—will have a pattern of scrub marks on its terminals that is not uniform.

Moreover, uniform, regular scrub marks are more advantageous than irregular scrub marks. This is because scrub marks on terminals of a semiconductor device can cause several problems. First, scrub marks can prevent a wire from being bonded to a terminal. (The terminals of a semiconductor device are often connected to conductors of a protective package by wires.) Second, even if a wire is successfully bonded to a terminal with a scrub mark, the scrub mark can decrease the effective life of the bond between the wire and the terminal. Third, a scrub mark can weaken a terminal, causing the terminal to loosen or even detach from the semiconductor device. (See U.S. Patent No. 5,506,499 to Puar ("Puar"), col. 2, lines 21-40 and col. 3, lines 7-25 for a discussion of the detrimental effects of scrub marks.) Increasing the uniformity of the scrub marks across terminals of a semiconductor device can reduce the

foregoing problems. For example, increasing the uniformity of the scrub marks typically prevents the formation of large scrub marks, which are particularly detrimental.

Indeed, the lack of uniformity in scrub marks left on a die by a probe card assembly that is not precisely planarized with the die is recognized in the industry as a problem, as evidenced by U.S. Patent No. 5,861,759 to Bialobrodski et al. ("Bialobrodski").<sup>1</sup> (See Bialobrodski col. 1, lines 14-23; col. 3, lines 23-33; and Figure 4.) That precisely planarizing the probes of the probe card assembly with the die produces a die that has generally uniform scrub marks and is therefore different and better than a prior art die tested with a probe card assembly that is not precisely planarized with the die is known in the industry is also evidenced by Bialobrodski. (See Bialobrodski col. 3, lines 34-44.)

Applicants have thus come forward with evidence and argument that the tested semiconductor devices of independent claim 43 (and each of the dependent claims that depend, directly or indirectly, from claim 43) are structurally different than and superior to prior art semiconductor devices, including the semiconductor devices disclosed in Littlebury. Applicants therefore assert that the pending claims are patentable over Littlebury.

Claim 82 includes a similar "adjusting a planar orientation" feature and therefore also produces a tested semiconductor device with generally uniform scrub marks from terminal to terminal. Claim 82 is therefore patentable for generally the same reasons as claim 43.

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<sup>1</sup> Applicants note that Bialobrodski, which was not filed until January 29, 1997, is not prior art to the present application, which claims priority through a chain of continuation and divisional applications to U.S. Patent No. 5,974,662, which was filed on November 9, 1995.

Appl. no. 10/034,528  
Amtd. dated June 6, 2006  
Reply to Office Action of January 6, 2006

In view of the foregoing, Applicants submit that all of the claims are allowable and the application is in condition for allowance. If the Examiner believes that a discussion with Applicants' attorney would be helpful, the Examiner is invited to contact the undersigned at (801) 323-5934.

Respectfully submitted,

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## Exhibit 1

Figure A

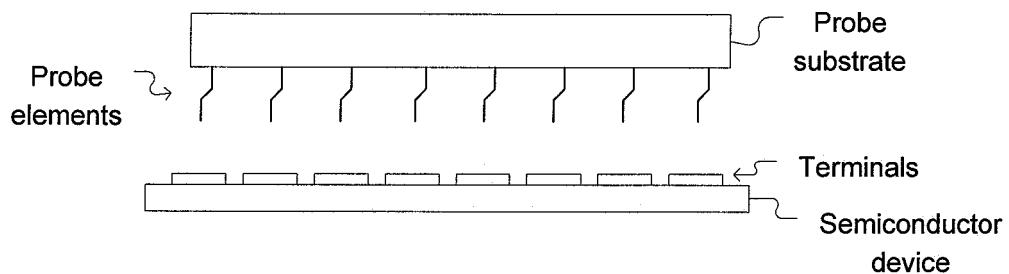


Figure B

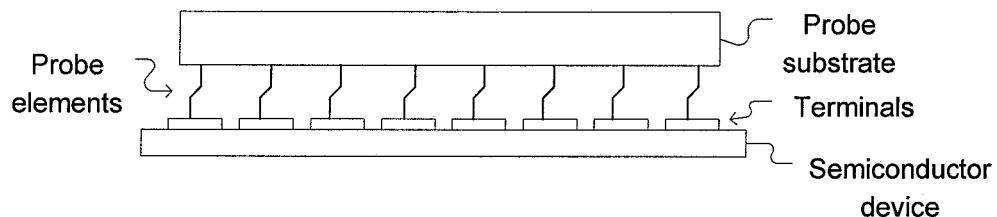


Figure C

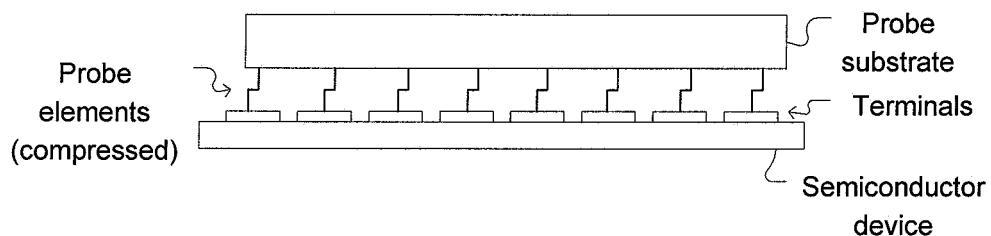
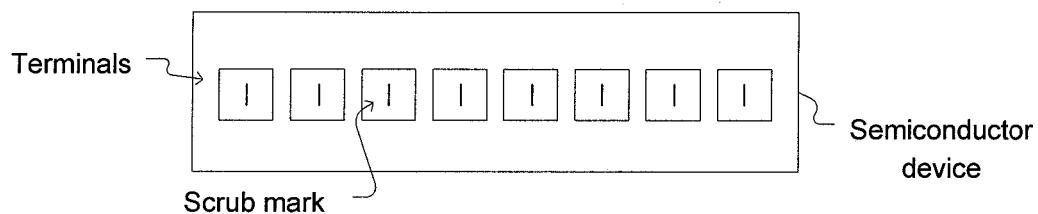


Figure D

(Top View)



## Exhibit 2

Figure E

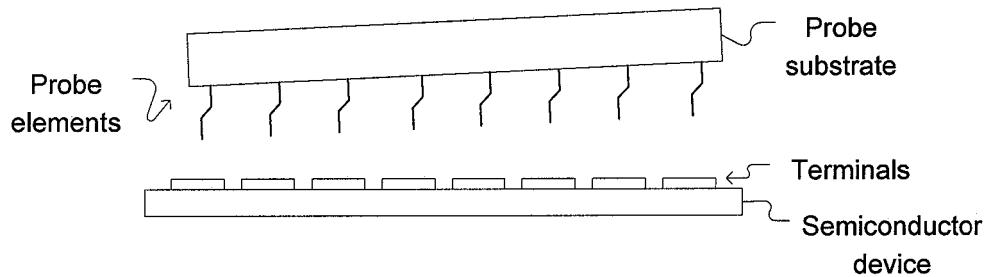


Figure F

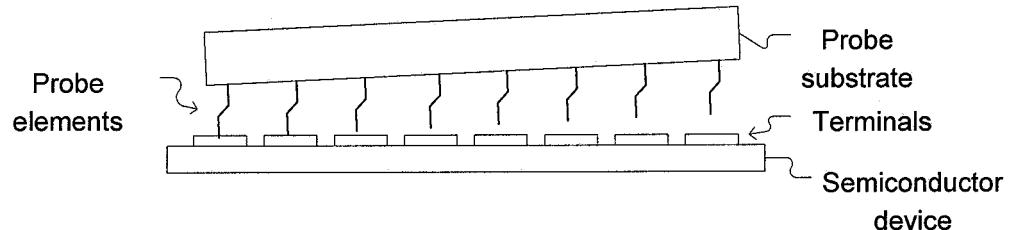


Figure G

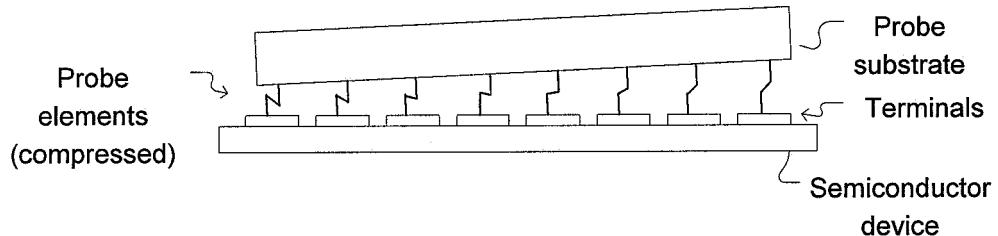


Figure H

(Top View)

